REMARKS

Claims 1-2, 4, and 8-20 are pending. Applicants have carefully considered the Office Action dated December 22, 2006 ("Office Action") in this Application. Applicants present the above amendments and following remarks in a sincere attempt to place this Application in condition for allowance. Applicants have cancelled Claims 3 and 5-7 in this Response. Applicants have amended Claims 1, 4, and 8-10 in this Response. Applicants have added New Claims 11-20 in this Response. Applicants respectfully request reconsideration and allowance in light of the above amendments and the following remarks.

Applicants wish to thank the Examiner for the courtesy of a telephone interview conducted on March 21, 2007. During the interview, the above amendments were discussed.

Applicants have amended the Specification in this Response to correct a minor informality. Applicants respectfully submit that no new matter is introduced as a result of this amendment.

Claims 3, 4, and 8 stand objected to for minor informalities. Applicants have corrected the identified informalities (and cancelled Claim 3) in this Response. Accordingly, Applicants respectfully request that the objections to the Claims be withdrawn.

Claims 1-2, 5, and 7-10 stand rejected under 35 U.S.C. §112, second paragraph, as allegedly indefinite. *See* Office Action, Page 2. In particular, the Examiner rejected Claim 1 for reciting, "a first processor means for providing said first processor means with access". Office Action, Page 2. Applicants have amended Claim 1 in this Response to recite, in relevant part, "A method, for use in a computer system having a main memory and a first processor, for providing said ***first*** processor with access. . ." (emphasis added). Applicants therefore respectfully request that this rejection be withdrawn.

Regarding Claims 5 and 7-10, the Examiner stated, "It is unclear what is meant by 'parameters'" in the claim element, "parameters of said specified program in said pool of memory." Office Action, Page 3. Applicants have cancelled Claims 5-7 in this Response. Applicants have amended Claims 8-10 in this Response to recite, in relevant part, "said register states embodying program parameters." Accordingly, Applicants therefore respectfully request that the rejections of Claims 1-2, 5, and 7-10 under 35 U.S.C. §112, second paragraph, be withdrawn.

Claims 1-4 and 8-10 stand rejected under 35 U.S.C. §103(a) as allegedly unpatentable over U.S. Patent No. 6,625,749 by Quatch ("Quatch") in view of U.S. Patent No. 5,491,787 by Hashemi ("Hashemi"). Applicants respectfully traverse these rejections.

The obligations of the Examiner in support of obviousness rejections are clearly defined at M.P.E.P. §2142: "The examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness" and "If the examiner does not produce a *prima facie* case, the applicant is under no obligation to submit evidence of non-obviousness." M.P.E.P. §2143 sets out the three basic criteria that a patent examiner must satisfy to establish a *prima facie* case of obviousness:

> 1. some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings;
> 2. a reasonable expectation of success; and
> 3. the teaching or suggestion of all the claim limitations by the prior art reference (or references when combined).

In the absence of a sufficient *prima facie* showing of obviousness by the Examiner (assuming there are no objections or other grounds for rejection), an applicant is entitled to grant of a patent. *See In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443 (Fed. Cir. 1992). Thus, in order to support an obviousness rejection, the Examiner is obliged to produce evidence compelling a conclusion that each of the three aforementioned basic criteria has been met.

In this case, Applicants respectfully submit that the Examiner has failed to produce evidence compelling a conclusion that the criteria required for a prima facie showing of obviousness has been met. In particular, Applicants respectfully submit that the Examiner's proposed combinations fail to teach each and every limitation in the Claims, as originally drafted, and especially as amended.

First, Claims 1, 4, and 8-10 have been amended to recite, in relevant part: "subsequent to storing said register states and accessing said register states, inspecting said register states for errors," and "subsequent to transmitting said register states, inspecting said register states for errors." Support for these amendments can be found, among other places, at Page 6, line 9 to Page 7, line 14 of the Original Application. Applicants respectfully submit that Quach affirmatively negates this element of amended Claims 1, 4, and 8-10.

Specifically, Quach states:

> The contents of the data register files are checked 420 for parity errors. ***If no parity error is found 430, the contents of the data register files are copied*** 440 to a specified memory location. As noted above, this may be a memory location shared with the other execution core or it may be a memory location reserved for particular execution core. ***If a parity error is found 430, no data is copied*** from the data register files. Alternatively, only uncorrupted data may be copied from the data register file(s).

Quach, col. 10, lines, 21-29 (emphasis added). Clearly, the data in Quach is inspected before copying, which directly and irreconcilably conflicts with the unique combinations recited in amended Claims 1, 4, and 8-10.

Additionally, there are other significant differences between the unique combinations recited in amended Claims 1, 4, and 8-10. For example, Quach clearly teaches switching modes in the Examiner's purported "supplemental processor", not "ceasc[d]", "operationally interrupted", or "halt[ed]" as recited in the Claims. Specifically, Quach teaches switching the processors into a "split mode," wherein "each execution core may independently execute the data recovery operations

of ERR." Quach, col. 9, lines 36-39. As such, Quach here, too, clearly teaches away from the unique combinations recited in Claims 1, 4, and 8-10.

Therefore, for at least the above reasons, Applicants respectfully submit that the Examiner's proposed combination fails to teach each and every element as recited in the Claims. Applicants therefore also respectfully submit that amended Claims 1, 4, and 8-10, and their dependent Claims, are therefore allowable over the cited art and the remaining art of record, in any combination.

Furthermore, Applicants have added new Claims 11-17 in this Response. Applicants respectfully submit that new Claims 11-17 are also allowable over the cited art for at least some of the same reasons that Claims 1, 4, and 8-10 are allowable over the cited art. For example, independent Claims 11 and 15 recite, in relevant part, "activating a debugging program on a main processing unit (MPU) of the computer system, the MPU inoperable to access registers of the SPU directly", "verifying, by the debugging program, that the first computer program is halted"; and "subsequent to accessing the SPU register contents, inspecting the SPU register contents for errors."

As described above, Applicants respectfully submit that these elements cannot be found anywhere in the cited art, in any combination. Therefore, Applicants respectfully submit that new Claim 11 and 15, and their associated dependent Claims 12-14 and 16-17 are also allowable over the cited art. Applicants therefore respectfully request allowance of new Claims 11-17.

Claims 5-7 stand rejected under 35 U.S.C. §103(a) as allegedly unpatentable over U.S. Patent No. 7,124,404 by Bebout et al. ("Bebout") in view of "Wikipedia's RAM" ("Wikipedia") and/or U.S. Patent Publication No. 2004/0207630 by Moreton ("Moreton"). Applicants respectfully traverse these rejections.

First, Applicants respectfully note that Claims 5-7 are cancelled in this Response.

Second, Applicants have added new Claims 18-20 in this Response. Applicants respectfully submit that new Claims 18-20 are clearly and precisely patentable over the cited art in any combination. Specifically, new Claim 18 recites, in relevant part:

> A debugging system, comprising: a debugging program *operational on a main processing unit (MPU)* of a computer system . . . a specialized function processing unit (SPU) coupled to the MPU and the main memory, *wherein the MPU is inoperable to access registers of the SPU directly* . . a copy program operational on the SPU . . . wherein the copy program on the SPU is configured to: transfer SPU register contents to an allocated portion of the main memory . . . wherein the debugging program on the MPU is further configured to: allocate a portion of a main memory of the computer system to store received SPU register contents; verify that the target computer program is halted; activate, on the SPU, the copy program; access the SPU register contents from the allocated portion of the main memory; [and] subsequent to accessing the SPU register contents, to inspect the SPU register contents for errors."

(Emphasis added.) Applicants respectfully submit that nowhere do the cited references, particularly Bebout, Wikipedia, and Moreton, in any combination, teach, disclose, or suggest the unique combination as recited in new Claim 18. Specifically, nowhere do the cited reference teach a debugging program operational on an MPU, wherein the MPU is inoperable to access registers of an SPU directly, with a copy program operational on the SPU configured to copy the SPU register contents to main memory, wherein the debugging program can access and modify the SPU register contents in main memory.

Instead, Bebout teaches a system using two debuggers, wherein "user commands", such as run, stop, or step, are converted to "debugger remote procedure calls (RPCs)", and intercepted by a "scheduler." *See* Bebout, col. 2, lines 54-64. The intercepted RPCs are then executed by *both* debuggers. *See* Bebout, col. 2, lines 64-66. In contrast, as recited in Claim 18, a *copy program* operational on the SPU copies the SPU register contents to main memory, and the debugging program can access and modify the SPU register contents *in main memory*. As recited in the Claims and the Specification, the copy program does not execute the debugging "user commands",

which are executed by the debugging program. Neither of the Examiner's other references, the Wikipedia and Moreton, show this unique combination, either.

Accordingly, Applicants respectfully submit that Claim 18 and its dependent Claims 19-20 are clearly patentable over Bebout and the remaining references of record, in any combination. As such, Applicants respectfully request allowance of Claims 18-20.

Applicants have now addressed all of the Claim objections and rejections cited in the Office Action. In view of the amendments to the Claims and Applicants' remarks, Applicants believe that pending Claims 1-2, 4, and 8-20 are in condition for allowance, and respectfully request allowance of Claims 1-2, 4, and 8-20.

Applicants believe no additional fees are due in this Response. In the event that any other fees are due, Applicants hereby authorize the Commissioner to charge any required fees due (other than issue fees), and to credit any overpayment made, in connection with the filing of this paper to Deposit Account No. 09-0447 of IBM Corporation.

Applicants believe that the present Response contains a complete response to the issues raised in the Office Action. Applicants respectfully request full reconsideration. If the Examiner should have any questions, comments or suggestions, the undersigned attorney earnestly requests a telephone conference. In particular, should the Examiner deem that any further amendment is desirable to place this application in condition for allowance, Applicants invite the Examiner to telephone the undersigned at the number listed below.

Respectfully submitted,

CARR LLP

Dated: March 22, 2007

/Gregory W. Carr/
Gregory W. Carr
Reg. No. 31,093

CARR LLP
670 Founders Square
900 Jackson Street
Dallas, Texas 75202
Telephone: (214) 760-3030
Fax: (214) 760-3003